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Xuancong Fan,[1,2] Renqiang Zhu,[2] Haowen Luo,[1,2] Jialun Li,[2] Hui Guo,[2] Yuanzhi He,[2] Kei May Lau,[2,a)] and Huaxing Jiang[1,a)]

AFFILIATIONS

[1]School of Integrated Circuits, South China University of Technology, Guangzhou, China
[2]The Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong SAR, China

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[a)]**Authors to whom correspondence should be addressed:** eekmlau@ust.hk and hxjiang@scut.edu.cn

ABSTRACT

In this paper, we report enhanced high-voltage blocking capability and improved gate dielectric reliability in vertical GaN-on-GaN trench metal–oxide–semiconductor field-effect transistors (MOSFETs) through fabrication process optimization. A thick bottom dielectric (TBD) is introduced at the trench bottom to suppress the peak electric fields in both the gate dielectric and the GaN layer, resulting in a substantial improvement in breakdown voltage (V_{BR}). The fabricated fully vertical device exhibits a low specific on-resistance ($R_{ON,sp}$) of 1.46 mΩ cm^2, a maximum drain current density ($I_{D,max}$) of 2.5 kA/cm^2, an on/off current ratio (I_{ON}/I_{OFF}) of 10^{10}, and a V_{BR} of 800 V, thereby achieving a competitive Baliga's figure of merit of 438 MW/cm^2. In addition, due to the increased gate-drain distance, the output capacitance (C_{OSS}) of the device is reduced by more than 14%, which is beneficial for reducing the switching loss. Reliability measurements, including positive bias threshold voltage instability and step-stress gate breakdown tests, indicate that the TBD improves the voltage tolerance of the gate dielectric without introducing additional instability at the channel interface. Interface trap density (D_{it}) at the trench sidewall is characterized by the conductance method, which is found to be 1×10^{12} cm^{-2} eV^{-1}. Furthermore, trap-assisted tunneling analysis of the gate leakage extracts a trap level of ∼1.3 eV within the Al_2O_3 gate dielectric, which accounts for the wear-out behavior under step-stress breakdown. This work demonstrates the effectiveness of the TBD technique for the development of high-performance and reliable GaN trench MOSFETs.

Vertical GaN transistors have attracted significant interest for power electronics due to their high-voltage capability and large current-handling capacity. Compared with lateral devices, vertical architectures can achieve high breakdown voltages (V_{BR}) without increasing chip area. In recent years, extensive research efforts have been devoted to various vertical GaN device concepts, including GaN trench metal–oxide–semiconductor field-effect transistors (MOSFETs),[1–6] current aperture vertical electron transistors (CAVETs),[7–9] *in situ* oxide, GaN interlayer-based vertical trench MOSFETs (OG-FETs),[10,11] and vertical GaN fin MOSFETs.[12–14] Among these approaches, GaN trench MOSFETs offer several advantages, such as a high threshold voltage (V_{TH}) that suppresses false turn-on, a relatively simple fabrication process that does not require regrowth or ion implantation, and potential avalanche capability enabled by the intrinsic p–n junction.

When fabricated on low-cost foreign substrates such as silicon[5,15,16] and sapphire,[3,17–19] quasi-vertical GaN trench MOSFETs are limited by the thickness of the drift layer, leading to a relatively low V_{BR}. In addition, current crowding effects further increase the on-resistance. Recently, fully vertical GaN trench MOSFETs on SiC and Si substrates incorporating conductive buffer layers have been successfully demonstrated, achieving breakdown voltages of 334 and 1200 V, respectively.[20,21] However, these devices exhibited relatively high on-resistance. In contrast, homoepitaxial MOSFETs on GaN bulk substrates[3,17–27] allow the growth of thick drift layers for high V_{BR}, while the absence of a buffer layer helps reduce the on-resistance.

For trench-type power devices, electric-field crowding at the trench corners in the off-state is a primary cause of premature gate-drain breakdown. Several approaches, such as trench field rings[28] and thick bottom dielectric (TBD),[29–34] have been proposed to alleviate

this field concentration. However, the influence of TBD integration on inversion-channel GaN-on-GaN trench MOSFETs has not been comprehensively investigated, particularly in terms of leakage mechanisms, interface trap effects, and device reliability. In addition, the impact of TBD on capacitance-related characteristics, such as output capacitance (C_{OSS}) reduction, has been extensively studied in SiC[32] devices but remains insufficiently explored in GaN trench MOSFETs.

In this work, we systematically investigate the impact of a TBD on the electrical and reliability performance of vertical GaN-on-GaN trench MOSFETs. By incorporating a TBD at the trench bottom, the electric-field distribution is effectively modulated, leading to suppression of the peak electric field at the trench corners and a pronounced enhancement in V_{BR}. The fabricated device exhibits a V_{TH} of 3.1 V, an on/off current ratio (I_{ON}/I_{OFF}) of 10^{10}, a maximum drain current density ($I_{D,max}$) of 2.5 kA/cm^2, a low specific on-resistance ($R_{ON,sp}$) of 1.46 mΩ cm^2, and a high V_{BR} of 800 V, corresponding to a Baliga's figure of merit [BFOM $= (V_{BR})^2/R_{ON,sp}$] of 438 MW/cm^2. In addition, the TBD design reduces the C_{OSS} by more than 14%, which is beneficial for switching performance. Reliability characterization, including positive bias threshold voltage instability (PBTI) and step-stress gate breakdown measurements, demonstrates improved gate dielectric robustness with TBD integration. The interface trap properties at the trench sidewall are further investigated by C–V measurements and physical modeling. Temperature-dependent measurements indicate that trap-assisted tunneling (TAT) dominates the gate leakage. These results provide a comprehensive understanding of TBD-based vertical GaN trench MOSFETs.

The epitaxial structure of the vertical GaN trench MOSFETs was grown on a 2-in. n-type GaN substrate. From bottom to top, the epitaxial stack consists of a 0.5-μm n$^+$-GaN layer [Si: 5×10^{18} cm^{-3}], a 9-μm n$^-$-GaN drift layer [Si: 5×10^{16} cm^{-3}], a 400-nm p-GaN layer, a 200-nm n$^+$-GaN layer [Si: 5×10^{18} cm^{-3}], and a 20-nm n^{++}-GaN layer [Si: 1×10^{19} cm^{-3}]. Figure 1(a) illustrates the schematic structure of the vertical GaN trench MOSFET. The Mg concentration in the p-GaN layer was tuned to 4×10^{18} cm^{-3}, as confirmed by secondary ion mass spectrometry (SIMS) depth profiling [Fig. 1(b)]. Compared with our previous work,[17] the Mg concentration was reduced from 10^{19} to 10^{18} cm^{-3} to improve the on-state performance. Figures 1(c) and 1(d) show the atomic force microscopy (AFM) and x-ray diffraction (XRD) characterization results of the as-grown wafer. The top n$^+$-GaN surface exhibits a low root mean square roughness of 0.61 nm, indicating excellent surface smoothness. Owing to the homoepitaxial growth on a GaN bulk substrate, the full width at half maximum (FWHM) values of the (002) and (102) rocking curves are 57 and 63 arc sec, respectively, which are significantly smaller than those typically observed in heteroepitaxial GaN layers. Based on established empirical relationships,[35] the threading dislocation density (TDD) is estimated to be on the order of 1×10^7 cm^{-2}, indicating high crystalline quality of the epilayers.

The fabrication of GaN-on-GaN trench MOSFETs either with or without a TBD followed a process flow similar to our previously reported work.[16,29] Trenches with a depth of 1.5 μm were formed using Cl_2/Ar inductively coupled plasma (ICP) etching with a SiO_2 hard mask. A low bias power of 5 W and a chamber pressure of 6 mTorr were employed to obtain smooth trench sidewalls with rounded bottom corners, which helps suppress off-state electric-field crowding at the trench corners. The p-contact and mesa regions were subsequently defined by ICP etching, followed by tetramethylammonium hydroxide (TMAH) treatment at 80 °C to mitigate etching-induced damage. The sample was then annealed at 800 °C for 20 min in N_2 to activate the p-GaN layer. Prior to the deposition of the Al_2O_3 gate dielectric, the trench sidewalls were cleaned using a piranha solution followed by buffered oxide etchant (BOE) to reduce interface trap density.[20,29] A 70-nm-thick Al_2O_3 gate dielectric was then deposited by thermal atomic layer deposition (ALD) at 300 °C. Ni/Au and Ti/Al/Ni/Au metal stacks were deposited as the p-contact and source electrodes, respectively. For the trench MOSFET incorporating a TBD, the trenches were first filled with ethylene–octene copolymer (EOC, from Everlight Chemical) before sputtering Ti/Cu/Au gate metal.[29] An O_2 plasma etch-back process was then used to retain a 750-nm-thick EOC layer at the trench bottom, forming the TBD, as illustrated in Fig. 2(a). The selected EOC thickness reflects a trade-off between electric-field modulation at the trench corner and the physical constraints of the device epitaxial layers (220 nm n$^+$-GaN source and 400 nm p-GaN body). Further optimization of the trench depth will be investigated in future work. Finally, a Ti/Al/Ni/Au metal stack was deposited on the backside of the sample to form the drain electrode. A top-view optical microscope image of the fabricated MOSFET is shown in Fig. 2(b).

The device features a single rectangular trench with a length of 100 μm and a width of 4 μm. In vertical GaN trench MOSFETs,[5,20] the electron current from the trench corner typically spreads laterally into the drift layer at an angle of approximately 45°. Considering the 9 μm drift-layer thickness, the effective area is estimated as $(4 + 9\,\mu\text{m}) \times (100 + 9\,\mu\text{m}) = 1417\,\mu\text{m}^2$. Figures 3(a) and 3(b) compare the transfer and output characteristics, respectively, for the devices with and without TBD. The V_{TH}, defined at a drain current density (I_D) of 1 A/cm^2, is 2.8 V for the device without TBD and 3.1 V for the device with TBD. Both devices exhibited a high I_{ON}/I_{OFF} of 10^{10} and a comparable gate current of $\sim 2 \times 10^{-5}$ A/cm^2 (at $V_{GS} = 15$ V). Upon introducing the TBD, the $R_{ON,sp}$ increased from 1.11 to 1.46 mΩ cm^2, while the $I_{D,max}$ decreased from 3027 to 2503 A/cm^2. This slight degradation in forward performance is attributed to EOC coverage along the trench sidewalls and bottom, which restricts carrier accumulation and increases resistance in the accumulation region.[29] Figure 3(c) shows the measured transfer curves with V_{BS} ranging from 2 to −3 V, where an increase in V_{TH} is observed as V_{BS} increases. The effective acceptor concentration (N_A) extracted using the body bias effect method[36] is $\sim 1 \times 10^{18}$ cm^{-3}. Since the anneal was performed after mesa and trench formation, leaving narrow p-GaN regions (5–44 μm) that provide highly efficient, short-distance pathways for lateral hydrogen out-diffusion, a relatively high activation rate of ~25% can be achieved.

Figure 4(a) compares the off-state leakage current of GaN-on-GaN trench MOSFETs with and without a TBD, alongside a test p–i–n diode fabricated on the same wafer. During the measurement, a V_{GS} of −5 V was applied to ensure complete channel depletion. The breakdown voltage, defined at I_D of 10 A/cm^2, was limited to 212 V for the device without TBD. In contrast, incorporating the TBD increased the V_{BR} to 800 V, nearly reaching the value of 864 V measured from the test p–i–n diode. A sharp increase in gate leakage occurs exactly at V_{BR}, indicating that the device failure is governed by destructive gate dielectric breakdown. At low drain biases, the device with the TBD actually exhibited lower drain and gate leakage than the

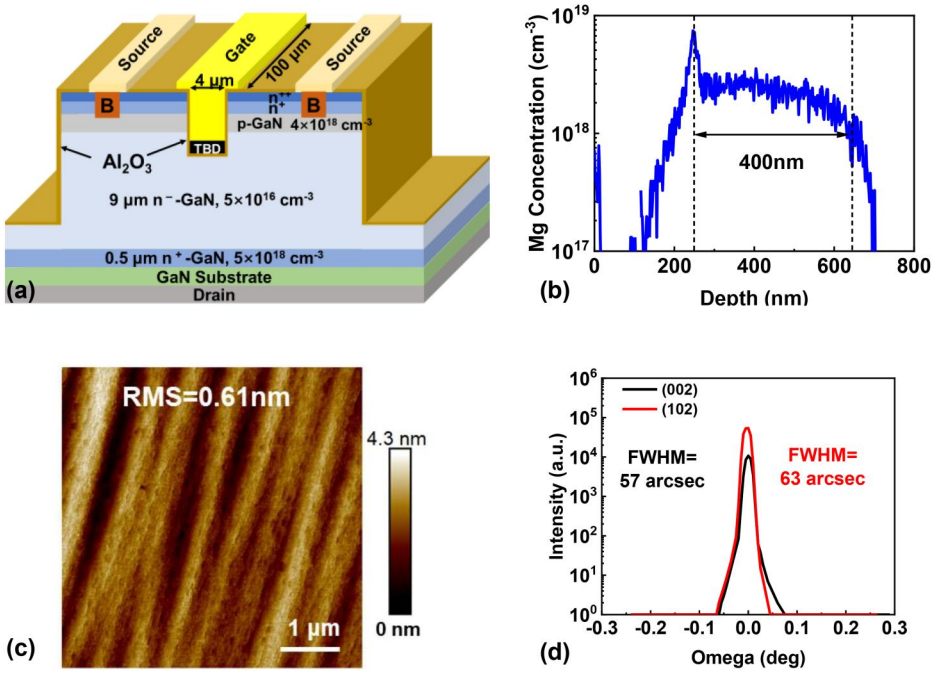

FIG. 1. (a) Cross-sectional schematic of the fully vertical GaN-on-GaN trench MOSFET with TBD. (b) SIMS depth profiling results of Mg concentration in the p-GaN layer. (c) AFM scan image and (d) XRD rocking curves of (002) and (102) planes of the as-grown wafer.

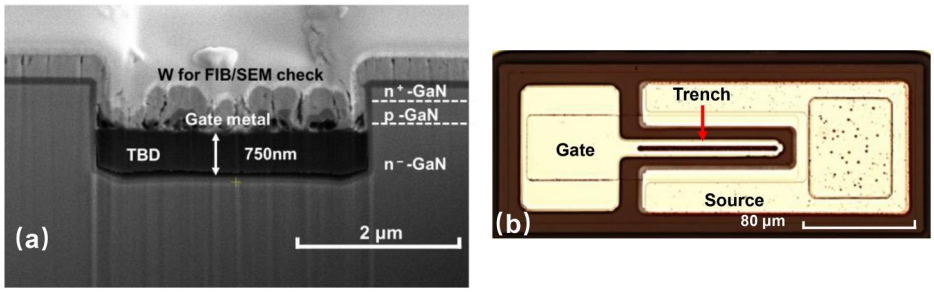

FIG. 2. (a) Cross-sectional SEM image of the gate trench region with EOC as the TBD layer. (b) Top-view optical microscope image of the fabricated MOSFET.

control device. This can be attributed to TBD coverage along the trench sidewalls and bottom, which strengthens the depletion effect and suppresses local carrier accumulation. As the drain voltage increased to approximately 200 V, field-enhanced leakage mechanisms began to dominate, diminishing the TBD's suppression effect and causing the leakage currents of both devices to converge. To further verify the effectiveness of the TBD in suppressing electric-field crowding, a statistical distribution of the measured V_{BR} is provided in Fig. 4(b). Despite this destructive testing constraint, the measured results demonstrate excellent uniformity across the tested samples. The significantly higher leakage current observed in the MOSFET compared to the reference p–i–n diode is most likely associated with the non-ideal nature of the Ni/p-GaN contact, which is unable to effectively clamp the body potential, leading to a floating body effect.

To quantify the interface trap properties at the trench sidewall, frequency-dependent conductance measurements were performed on both devices (with and without TBD) near the V_{TH}. The interface trap density (D_{it}) and trap energy level $E_C - E_T$ were extracted from the equivalent parallel conductance G_P/ω peaks measured at frequencies from 10 kHz to 1 MHz using the standard Shockley–Read–Hall (SRH) statistics as described in the following equations:[37,38]

$$\frac{G_P}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln\left[1 + (\omega\tau_{it})^2\right], \tag{1}$$

$$E_C - E_T = kT \ln(\tau_{it} \nu_{th} \sigma_n N_C), \tag{2}$$

where τ_{it} is the trap time constant. The values used for the trap capture cross section ($\sigma_n = 1 \times 10^{-15}$ cm^2), the thermal velocity ($\nu_{th} = 2 \times 10^7$ cm/s), and the effective density of states in the GaN conduction band ($N_C = 2.2 \times 10^{18}$ cm^{-3}) are adopted from Ref. 39.

As presented in Figs. 5(a) and 5(b), the measured G_P/ω vs ω data for both devices can be well fitted by the SRH analytical model. The analysis reveals a dominant interface trap energy level located at 0.24–0.27 eV below the GaN conduction band [Fig. 5(c)], which has been reported to be associated with dangling bonds at the dielectric/GaN interface,[40,41] O_N-related defect complexes,[42] and defect clusters at dislocation sites.[43] The extracted D_{it} values are approximately

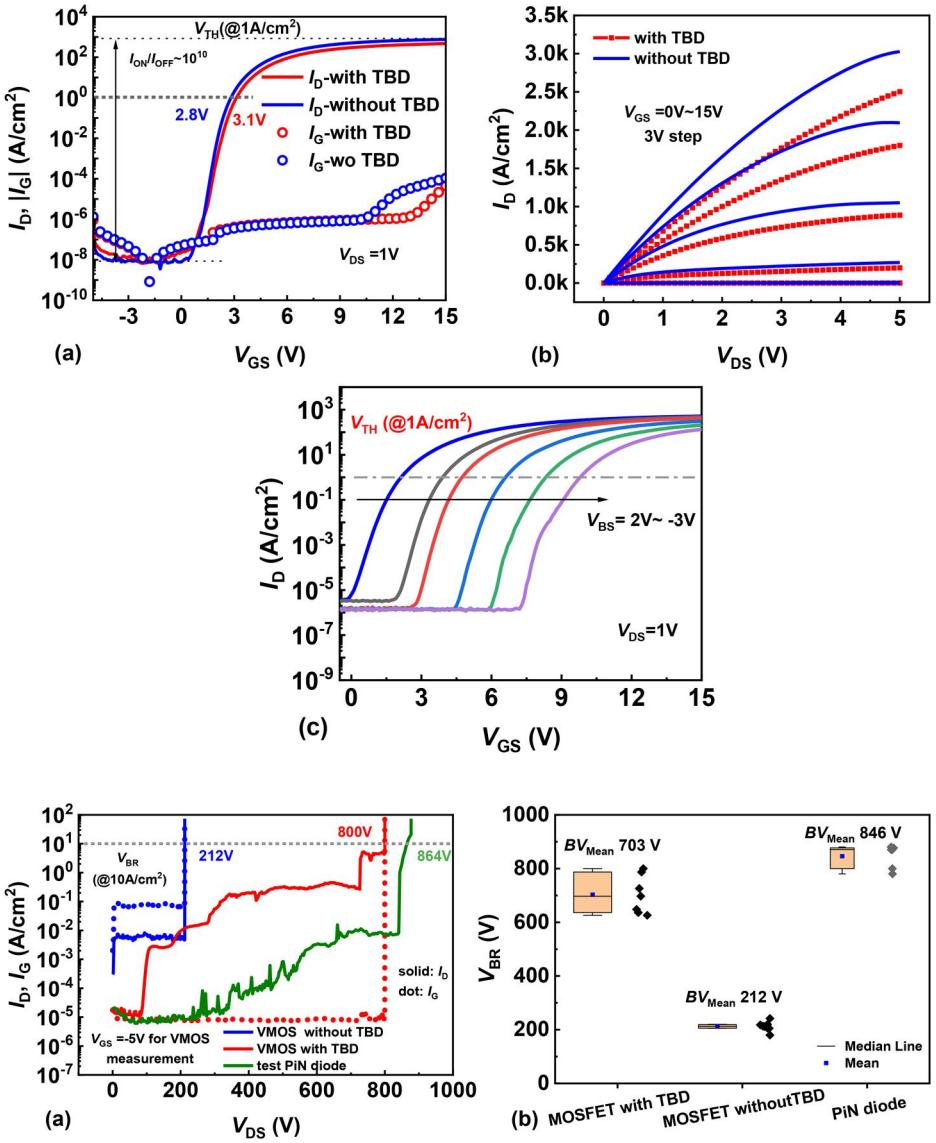

FIG. 3. (a) Transfer and (b) output characteristics of GaN-on-GaN trench MOSFETs with and without TBD. (c) Transfer characteristics of the fabricated MOSFET at V_{BS} from 2 to −3 V, used to extract N_A.

FIG. 4. (a) Off-state leakage currents and (b) statistical distribution of V_{BR} for vertical MOSFETs with and without TBD, as well as the test p–i–n diode on the same sample.

1×10^{12} cm^{-2} eV^{-1} for both the device with TBD and the control device. The comparable D_{it} values and identified trap energy levels provide critical insight into the nature of the trapping mechanisms. Specifically, they indicate that the introduction of the TBD and the associated EOC etch-back process do not induce additional defect generation along the trench sidewall interface.

Figure 6 presents TCAD-simulated electric-field distributions for the GaN trench MOSFETs at $V_{DS} = 800$ V and $V_{GS} = -5$ V. Figures 6(a)–6(c) compare the electric-field distributions in the Al_2O_3 gate dielectric for devices with and without a TBD, including cutline profiles at the trench bottom. Similarly, Figs. 6(d)–6(f) illustrate the electric-field distributions and cutline profiles within the GaN layer. In all cases, the peak electric field is located at the trench bottom corner. Without a TBD, the peak electric fields in Al_2O_3 and GaN reach 4.77 and 3.0 MV/cm, respectively. With the TBD, these values are significantly reduced to 1.97 and 1.8 MV/cm. These reductions confirm that the TBD effectively suppresses the peak electric field in both the dielectric and the semiconductor, accounting for the experimentally observed V_{BR} enhancement. Consequently, the device achieved a high V_{BR} of 800 V and a Baliga's figure of merit of 438 MW/cm^2.

Figure 7 presents the reliability test results of the fabricated devices. Figure 7(a) illustrates the PBTI stress waveform, and Fig. 7(b) shows the extracted ΔV_{TH} as a function of PBTI gate stress time. For both devices with and without TBD, a gradual positive shift in V_{TH} is observed with increasing stress time. This shift is attributed to progressive electron trapping at interface states and near-interface border traps. As the stress continues, more electrons are captured, resulting in an accumulation of trapped charge and a corresponding increase in V_{TH}. This indicates that the TBD integration does not introduce anomalous charge-trapping or instability. Figure 7(c) presents the

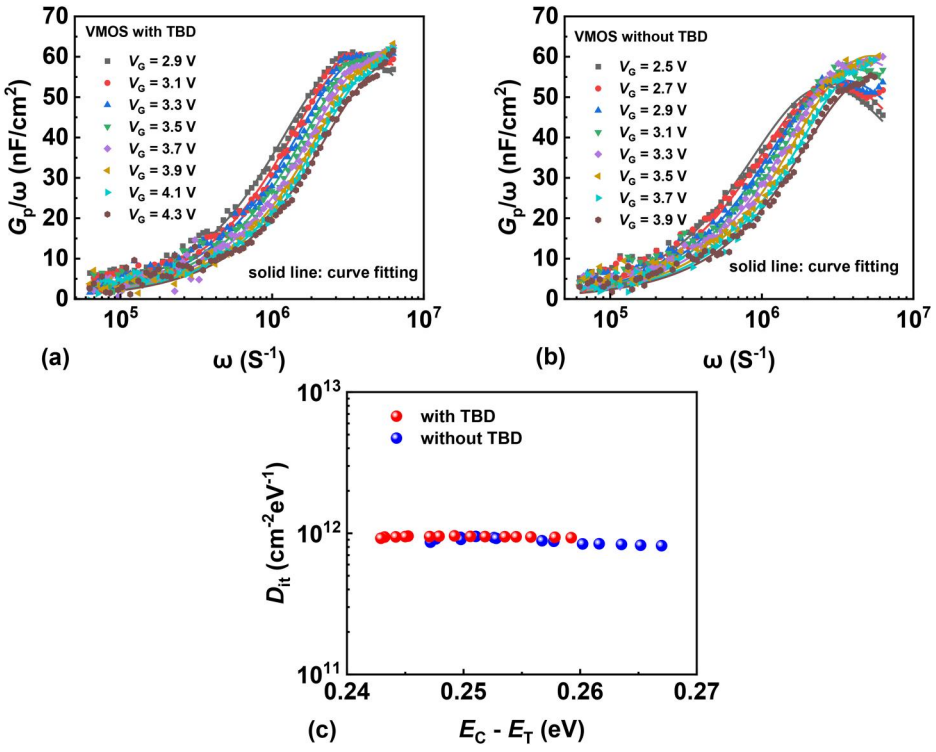

FIG. 5. Measured (symbols) and fitted (lines) G_P/ω as a function of angular frequency ω for the vertical GaN trench MOSFETs (a) with TBD and (b) without TBD. (c) Extracted interface trap density D_{it} vs trap energy level $E_C - E_T$ for both devices, obtained from the conductance method.

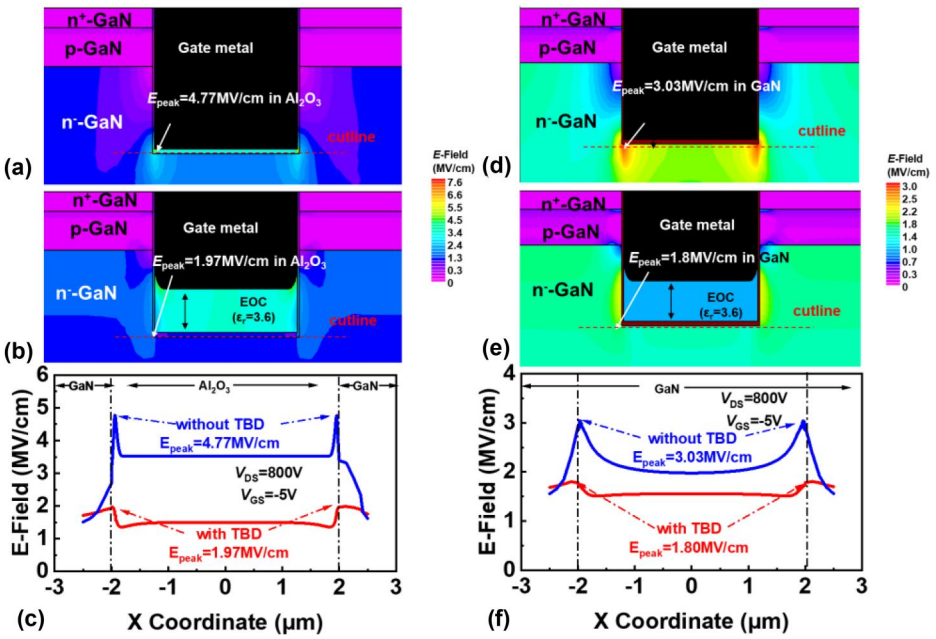

FIG. 6. TCAD simulation results of electric-field distribution of GaN trench MOSFETs at $V_{DS} = 800$ V, $V_{GS} = -5$ V. Electric-field distributions in the Al_2O_3 gate dielectric (a) without and (b) with the TBD. (c) Corresponding electric-field profiles in Al_2O_3 along the cutlines at the gate trench bottom. Electric-field distributions in the GaN region (d) without and (e) with the TBD. (f) Corresponding electric-field profiles in GaN along the cutlines at the gate trench bottom.

step-stressed forward gate breakdown characteristics. The gate stress voltage was increased from 1 to 29 V in steps of 4 V, with each step applied for 120 s, followed by constant stress at 29 and 31 V for 1200 s. The device without TBD sustained 29 V for 230 s and failed rapidly under higher stress, whereas the device with TBD exhibited improved endurance, sustaining 31 V for 82 s. This result indicates that the incorporation of TBD enhances the voltage tolerance and reliability of the gate dielectric.

To elucidate the physical mechanisms governing gate wear-out and dielectric failure, temperature-dependent gate leakage measurements

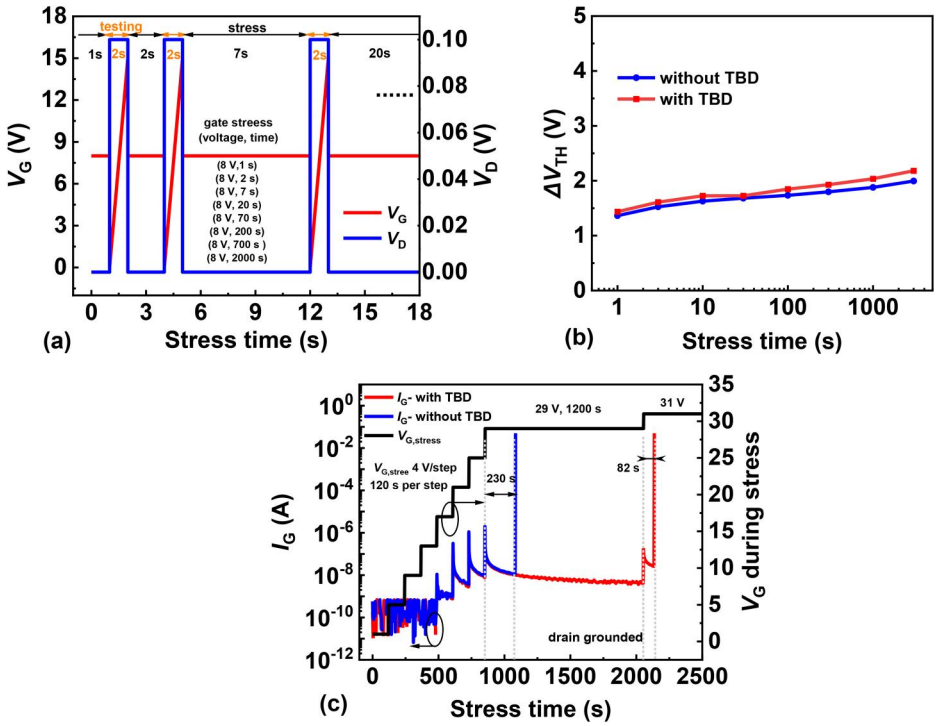

FIG. 7. Reliability characterization of vertical GaN trench MOSFETs with and without TBD. (a) Gate bias stress waveform applied during the PBTI measurement. (b) Extracted ΔV_{TH} vs stress time for devices with and without TBD. (c) Step-stressed forward gate breakdown characteristics.

were conducted on both devices (with and without TBD) from 25 to 150 °C. The leakage mechanisms were systematically analyzed using the TAT model, which is widely adopted in Al_2O_3/GaN MOS structures. Figures 8(a) and 8(c) show the gate current density (J_G) as a function of V_G for the devices with and without TBD, respectively. Notably, at the peak temperature of 150 °C, the control device (without TBD) exhibited premature gate breakdown at 18 V. This failure is driven by the enhanced local electric-field crowding at the trench corners, which is severely exacerbated by increased thermal carrier activity.

The TAT current density is described by the following expression:[44,45]

$$J_{TAT} \propto \exp\left(-\frac{8\pi\sqrt{2qm_{ox}}}{3hE_{ox}}\phi_t^{3/2}\right), \quad (3)$$

where h is Planck's constant, E_{ox} is the oxide electric field, $m_{ox} = 0.5\,m_e$ is the effective electron mass in Al_2O_3, and Φ_t is the trap energy level relative to the Al_2O_3 conduction band edge. As shown in Figs. 8(b) and 8(d), the $\ln(J_G)$ vs $1/E_{ox}$ plots exhibit excellent linearity over the entire temperature range, indicating that TAT is the dominant gate leakage mechanism. This indicates that carriers tunnel through the gate dielectric primarily via defect-assisted pathways rather than via Fowler–Nordheim tunneling (FNT) or Poole–Frenkel emission (PFE).

The trap energy level Φ_t can be extracted from the slopes of the $\ln(J_G)$ vs $1/E_{ox}$ plots [Figs. 8(b) and 8(d)]. For the device with TBD, the extracted Φ_t ranges from 1.1 to 1.3 eV, while the control device exhibits similar values ranging from 1.12 to 1.32 eV. These trap depths are consistent with vacancy-related defects and intrinsic traps previously reported in ALD Al_2O_3 films, which typically exhibit Φ_t values between 1.0 and 1.8 eV below the conduction band.[46,47] The nearly identical Φ_t values confirm that the TBD integration process does not introduce additional trap levels into the Al_2O_3 gate dielectric. This TAT-dominated leakage mechanism explains the physical wear-out process observed during step-stress breakdown. Under high-field stress conditions, TAT drives continuous charge injection into the Al_2O_3 bulk, progressively degrading the dielectric until catastrophic failure occurs.

The use of a TBD has been reported to effectively reduce C_{OSS} in trench MOSFET structures.[31,32] In this work, incorporating a TBD into GaN trench MOSFETs also led to a reduction in C_{OSS}. Under test conditions of $V_{DS} = 40$ V and f = 100 kHz (with grounded gate and source), the capacitance decreased from 2.12 to 1.81 pF upon the introduction of TBD, representing a 14.6% reduction, as shown in Fig. 9. The TBD weakens the electrostatic coupling between the gate and drain, thereby reducing C_{OSS}.

Figure 10 benchmarks the $R_{ON,sp}$ vs V_{BR} of our vertical GaN-on-GaN trench MOSFET with TBD to previously reported devices on different substrates. With a BFOM of 438 MW/cm^2, the device shows competitive performance relative to current state-of-the-art vertical GaN technology. Further performance enhancements may be realized through continued optimization of the epitaxial structure and fabrication processes, such as (i) increasing drift-layer thickness alongside optimized edge termination to further boost the V_{BR}, (ii) investigating the impact of trench depth on the performance of vertical GaN trench MOSFETs, and (iii) improving the p-GaN Ohmic contact.

In summary, vertical GaN-on-GaN trench MOSFETs incorporating a TBD have been demonstrated with significantly improved off-state performance and reliability. The TBD effectively suppresses electric-field crowding at trench corners, enhancing the V_{BR} to 800 V.

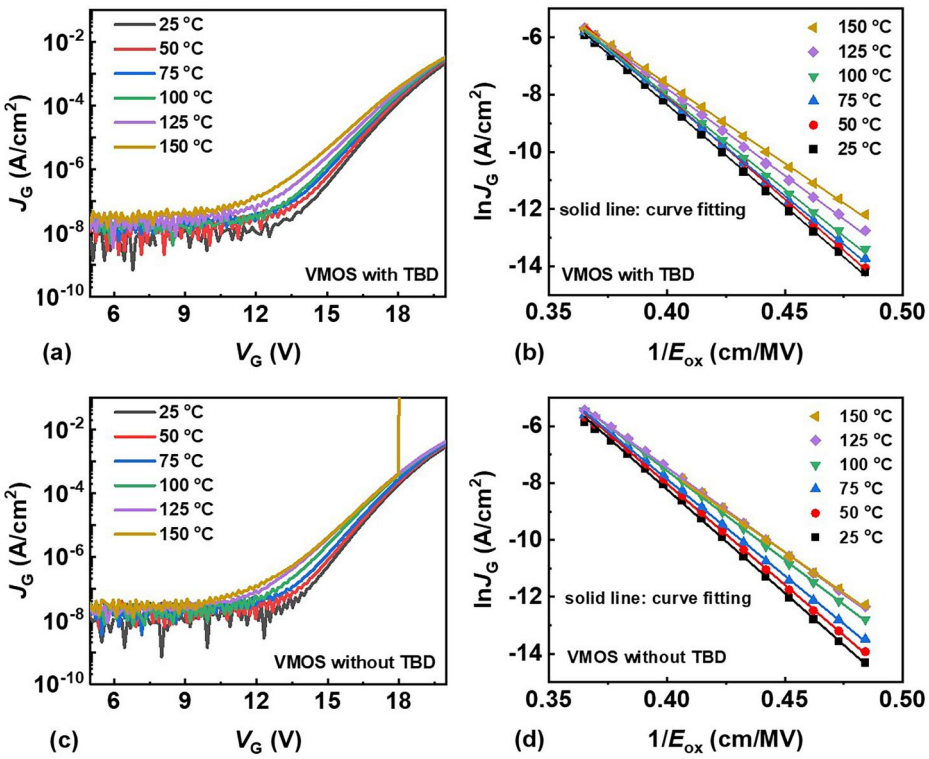

FIG. 8. (a) Gate leakage current density J_G as a function of V_G for the device with TBD (25–150 °C). (b) ln(J_G) vs 1/E_{ox} fitted using the TAT model for the device with TBD, yielding a Φ_t of 1.1–1.3 eV within the Al_2O_3 gate dielectric. (c) J_G vs V_G for the device without TBD. (d) ln(J_G) vs. 1/E_{ox} plot for the device without TBD, yielding a Φ_t of 1.12–1.32 eV.

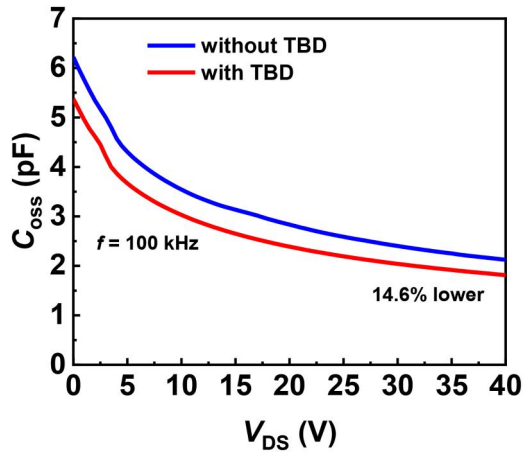

FIG. 9. C_{OSS}–V_{DS} characteristics of vertical GaN trench MOSFETs with and without TBD.

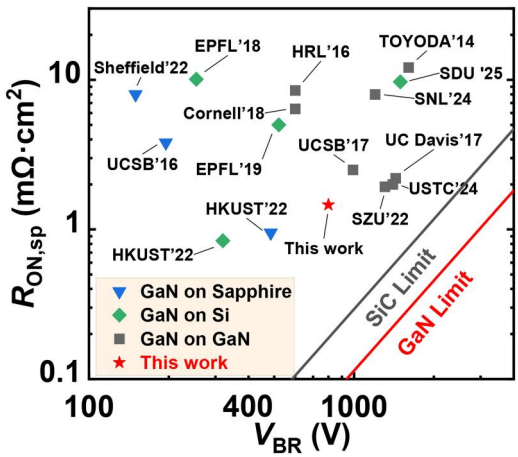

FIG. 10. $R_{ON,sp}$ vs V_{BR} benchmarking of the GaN-on-GaN trench MOSFETs in this work with other reported state-of-the-art vertical GaN trench MOSFETs.

The increased gate-drain separation reduces C_{OSS} by 14.6%, contributing to improved switching performance. The devices exhibit a low $R_{ON,sp}$ of 1.46 mΩ cm^2, an $I_{D,max}$ of 2.5 kA/cm^2, an I_{ON}/I_{OFF} of 10^{10}, and a high BFOM of 438 MW/cm^2, indicating a favorable trade-off between conduction and blocking performance. The conductance analysis reveals interface trap states at the trench sidewall with $E_C - E_T = 0.24$–0.27 eV and a density of about 1×10^{12} cm^{-2} eV^{-1}. In addition, TAT analysis identifies deeper trap states at 1.1 to 1.3 eV within the Al_2O_3 gate dielectric. Reliability measurements, including PBTI and step-stress gate breakdown, further confirm that the TBD improves the voltage tolerance of the gate dielectric without introducing additional instability at the channel interface. These results highlight the significant potential of TBD integration for advancing high-performance and reliable GaN power devices.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Xuancong Fan: Conceptualization (equal); Data curation (equal); Investigation (lead); Methodology (lead); Writing – original draft (lead). **Renqiang Zhu:** Conceptualization (equal); Methodology (equal); Validation (equal). **Haowen Luo:** Software (equal). **Jialun Li:** Methodology (supporting). **Hui Guo:** Formal analysis (supporting). **Yuanzhi He:** Data curation (supporting). **Kei May Lau:** Funding acquisition (lead); Resources (lead); Supervision (equal); Writing – review & editing (equal). **Huaxing Jiang:** Funding acquisition (equal); Resources (equal); Supervision (lead); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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